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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,311	03/31/2004	Nick Lindert	42P18257	9112

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,311	LINDERT ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 43-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43 and 51* is/are allowed.

6)☒ Claim(s) *1-10,12-19 and 44-50* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/11/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 10 is objected to because of the following informalities:

In claim 10, line 5, the term "said bulk semiconductor substrate" should be corrected to read, "said bulk silicon monocrystalline substrate".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 10, 12-15 and 44-45 and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (US 2003/0227036) in view of Yeo et al. (US 2005/0035415).

Regarding claim 1, Sugiyama et al. discloses in figure 2 a semiconductor device comprising:

a semiconductor body 30 (para [0075], line 4) on a semiconductor substrate 10, the semiconductor body having a top surface and laterally opposite sidewalls;

a semiconductor capping layer 40 (para [0075], line 6) formed on the top surface and on the sidewalls of said semiconductor body;

a gate dielectric layer 70 (para [0076], line 3) formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body;

a gate electrode 80 (para [0076], line 1) having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer;

a pair of source/drain regions 50, 60 (para [0076], line 6) formed in said semiconductor body on opposite sides of said gate electrode.

It is noted that element 40 is construed as "capping layer" since it constitutes a similar structure and functions as the claimed capping layer.

Sugiyama et al. does not disclose a semiconductor body on an active region of a bulk semiconductor substrate and an isolation region on said bulk semiconductor substrate, said isolation region adjacent to said active region. However, Yeo discloses in figure 3 a semiconductor body 134 on an active region of a bulk semiconductor substrate 132 and an isolation region 136 on said bulk semiconductor substrate, said isolation region adjacent to said active region. See paragraph [0032].

In view of such teaching, it would have been obvious at the time of the present invention to modify Sugiyama et al. by including a semiconductor body on an active region of a bulk semiconductor substrate and an isolation region on said bulk semiconductor substrate, said isolation region adjacent to said active region in order to electrically separate the gate from the semiconductor substrate and to scale the device at a significantly reduced cost due to the cheaper bulk silicon substrate (para [0012], lines 3-7, Yeo).

Regarding claim 2, Sugiyama et al. discloses in figure 2 said capping layer 40 has a tensile stress. Applicant teaches, "a single crystalline silicon film formed on a silicon germanium alloy semiconductor body 208 will cause the single crystalline silicon film to have a tensile stress" (para [0017] of the instant application). Sugiyama teaches the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium alloy semiconductor body 30 (para [0075]). Therefore, the capping layer 40 inherently has a tensile stress.

Regarding claim 3, Sugiyama et al. discloses in figure 2 the semiconductor-capping layer has greater tensile stress on the sidewalls of the semiconductor body than on the top surface of the semiconductor body. Applicant teaches, "the silicon capping layer formed on the sidewalls 322 of the silicon germanium alloy will witness a substantial tensile stress and a lower but significant tensile strain on the top surface 319 of the silicon germanium alloy" (para [0043]). Sugiyama teaches that the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium alloy semiconductor body 30 (para [0075]). Therefore, the semiconductor-capping layer inherently has greater tensile stress on the sidewalls of the semiconductor body than on the top surface of the semiconductor body.

Regarding claim 4, Sugiyama et al. discloses the source/drain regions are n type conductivity (para [0066]).

Regarding claim 5, Sugiyama et al. discloses the semiconductor substrate is a silicon substrate (para [0089]), wherein the semiconductor body is a silicon germanium alloy (para [0075]) and wherein the capping layer is a silicon film (para [0075]).

Regarding claim 10, Sugiyama et al. discloses in figure 2 a semiconductor device comprising:

a silicon germanium body 30 (para [0075], line 4) formed on a semiconductor substrate 10, said silicon germanium body having a top surface and a pair of laterally opposite sidewalls;

a silicon film 40 (para [0075], line 6) formed on said top surface and on said sidewalls of said silicon germanium body;

a gate dielectric layer 70 formed on said silicon film on said top surface of said silicon germanium body and on said silicon film on said sidewalls of said silicon germanium body;

a gate electrode 80 having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer;

a pair of source/drain regions 50, 60 formed in said silicon germanium body 30 on opposite sides of said gate electrode.

Sugiyama et al. discloses a silicon germanium body on a semiconductor substrate 10, not on an active region of a bulk silicon monocrystalline substrate and an isolation region on said bulk silicon monocrystalline substrate, said isolation region adjacent to said active region and adjacent to a portion of said body as recited in claim

10. However, Yeo discloses in figure 3 a semiconductor body 134 on an active region of a bulk silicon monocrystalline substrate 132 and an isolation region 136 on said bulk silicon monocrystalline substrate, said isolation region adjacent to said active region and adjacent to a portion of said body. See paragraph [0032].

In view of such teaching, it would have been obvious at the time of the present invention to modify Sugiyama et al. by including a body on an active region of a bulk silicon monocrystalline substrate and an isolation region on said bulk silicon monocrystalline substrate, said isolation region adjacent to said active region and adjacent to a portion of said body in order to electrically separate the gate from the semiconductor substrate and to scale the device at a significantly reduced cost because of the cheaper bulk silicon substrate (para [0012], lines 3-7, Yeo).

Regarding claim 12, Sugiyama et al. discloses on figure 2 the silicon film 40 has a thickness between 50-300A (para [0102]).

Regarding claim 13, Sugiyama et al. discloses on figure 2 the silicon germanium alloy comprises between 5-40% of germanium (para [0067]).

Regarding claim 14, Sugiyama et al. discloses on figure 22 the silicon germanium alloy comprises between 15-25% of germanium (para [0067]).

Regarding claim 15, Sugiyama et al. discloses that the source/drain regions are n type conductivity (para [0066]).

Regarding claim 44, similar to claim 1 above Sugiyama et al. discloses in figure 2 substantially all the structure set forth in claim 44. Sugiyama et al. further discloses the semiconductor body 30 is formed of SiGe (para 0075], line 4), which has a different lattice constant than said semiconductor substrate 10 formed of silicon (para [0072], lines 5-6).

Sugiyama et al. does not disclose a semiconductor body on an active region of a bulk semiconductor substrate and an isolation region on said bulk semiconductor substrate, said isolation region adjacent to said active region. However, Yeo discloses in figure 3 a semiconductor body 134 on an active region of a bulk semiconductor substrate 132 and an isolation region 136 on said bulk semiconductor substrate, said isolation region adjacent to said active region. See paragraph [0032].

In view of such teaching, it would have been obvious at the time of the present invention to modify Sugiyama et al. by including a semiconductor body on an active region of a bulk semiconductor substrate and an isolation region on said bulk semiconductor substrate, said isolation region adjacent to said active region in order to electrically separate the gate from the semiconductor substrate and to scale the device at a significantly reduced cost because of the cheaper bulk silicon substrate (para [0012], lines 3-7, Yeo).

Regarding claim 45, it is assumed that the semiconductor body formed of SiGe (para [0075], line 4), which has a lattice constant larger than the lattice constant of the bulk semiconductor substrate formed of silicon (para [0003], line 8, Liu).

Regarding claim 48, it is assumed that the semiconductor-capping layer 40 formed of silicon (para [0075], line 6, Sugiyama et al.), which has a lattice constant smaller than that of the semiconductor body 30 formed of SiGe (para [0075], line 4, Sugiyama et al.).

Regarding claim 49, Yeo discloses the bulk semiconductor substrate is a silicon substrate (para [0031], lines 9-10), wherein Sugiyama et al. discloses said semiconductor body 30 is a silicon germanium (para [0075], line 4) and the capping layer 40 is a silicon film (para [0075], lines 5-6).

Claims 6-9, 16-19, 46-47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. and Yeo in view of Liu (US 2004/0195624).

Regarding claims 6, 9,16 and 50, applicant teaches in para [0017], "a single crystalline silicon capping layer 210 formed on a silicon carbon alloy semiconductor body 208 will cause the single crystalline silicon film 210 to have a compressive stress". Sugiyama et al. teaches the capping layer 40 is a silicon layer (para [0075]), lines 5-6) formed on a silicon germanium (SiGe) alloy semiconductor body 30 (para [0075], line 4), not on a silicon carbon (SiC) alloy body. However, Liu et al. teaches in (para [0010])

either SiGe or SiC can be alternatively used as an alloy body Therefore, it would have been obvious to one of ordinary skill in the art at the time of the present invention to modify Sugiyama et al. and Yeo by including a silicon carbon alloy semiconductor body since the examiner takes Office Notice of the equivalence of SiGe and SiC for their use in a semiconductor body and the selection of any of these known equivalents would be within the level of ordinary skill in the art.

Regarding claim 7, Sugiyama et al. and Liu et al together disclose the semiconductor-capping layer has a greater compressive stress on the sidewalls than on the top surface of the semiconductor body. Note that Sugiyama et al. and Liu et al. together disclose a silicon capping layer is formed on a silicon carbon body, and it is assumed that a silicon capping layer formed on a silicon carbon body inherently constitutes this feature.

Regarding claim 8, Sugiyama et al. discloses the semiconductor substrate is a silicon substrate (para [0089]), wherein the capping layer is a silicon film (para [0075]), and Liu et al. discloses in (para [0010]) the semiconductor body comprises a silicon carbon alloy.

Regarding claims 17 and 18, Sugiyama et al. discloses the silicon film 40 has a thickness between 50-300A (para [0102], lines 6-7).

Regarding claim 19, Sugiyama et al. disclose the source/drain regions are p type (para [0077]). Note that Sugiyama teaches this structure can be manufactured for both p and n channel MISFET's (para [0077]).

Regarding claim 46, it is assumed that the semiconductor body formed of SiC will have a lattice constant smaller than that of the bulk semiconductor substrate formed of silicon, and Liu et al. teaches in para [0010] the semiconductor body is formed of SiC.

Regarding claim 47, it is assumed that the semiconductor-capping layer 40 formed of silicon (para [0075], lines 5-6, Sugiyama et al.) will have a lattice constant larger than that of the semiconductor body when the semiconductor body is formed of SiC, and Liu et al. teaches in para [0010] the semiconductor body is formed of SiC.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 43 and 51 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The reference (s) of record do not teach or suggest, either singularly or in combination at least the limitation of "said silicon film formed thicker on the top surface

of said silicon germanium body than on the sidewalls of said silicon germanium body" for claims 11 and 43, "said semiconductor capping layer is thicker on the top surface of said semiconductor body than on the sidewalls of said semiconductor body" for claim 51.

Response to Arguments

Applicant's arguments with respect to claims 1-10, 12-19 and 44-50 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

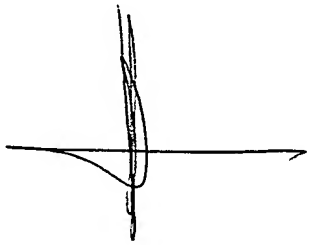
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
March 3, 2006.



KENNETH PARKER
SUPERVISORY PATENT EXAMINER